SVM Series

VMEbus-Based Switching Modules

User's Manual

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VXI Technology, Inc.

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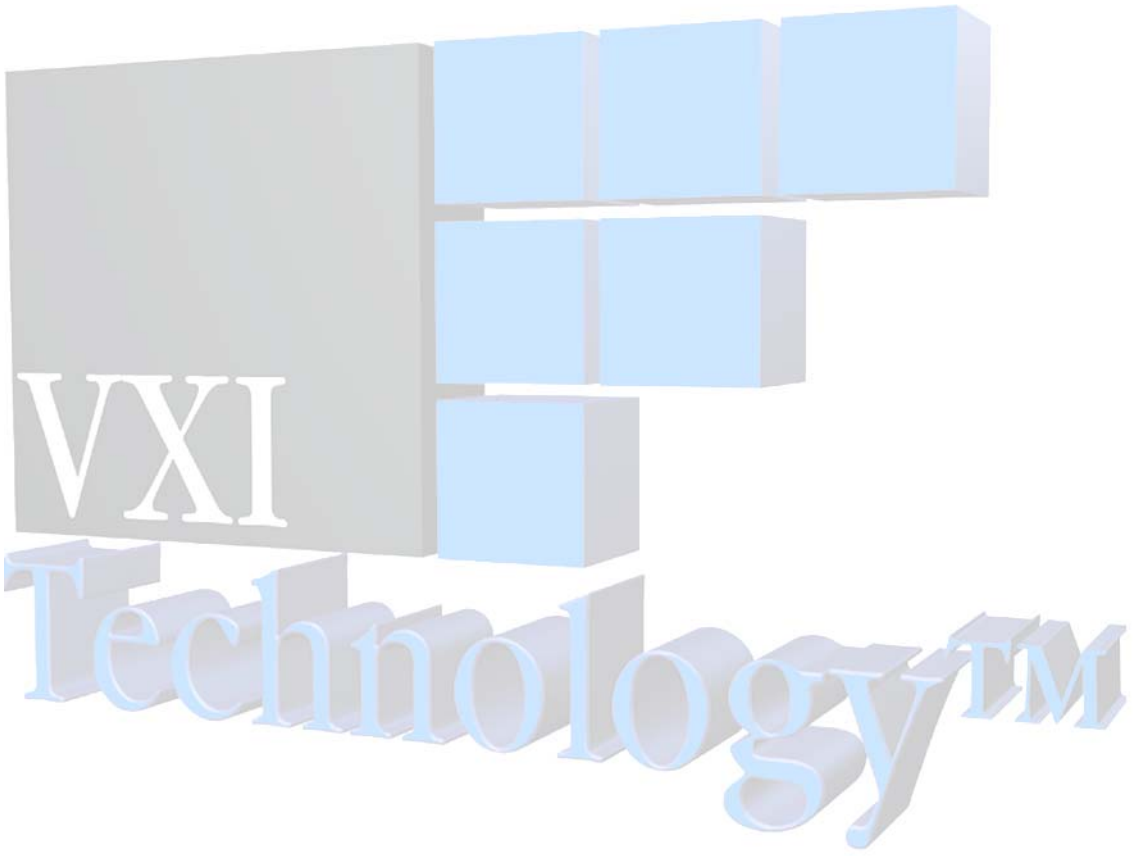
VXI
Technology™

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CERTIFICATION

VXI Technology, Inc. (VTI) certifies that this product met its published specifications at the time of shipment from the factory. VTI further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology (formerly National Bureau of Standards), to the extent allowed by that organization's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

The product referred to herein is warranted against defects in material and workmanship for a period of one year from the receipt date of the product at customer's facility. The sole and exclusive remedy for breach of any warranty concerning these goods shall be repair or replacement of defective parts, or a refund of the purchase price, to be determined at the option of VTI.

For warranty service or repair, this product must be returned to a VXI Technology authorized service center. The product shall be shipped prepaid to VTI and VTI shall prepay all returns of the product to the buyer. However, the buyer shall pay all shipping charges, duties, and taxes for products returned to VTI from another country.

VTI warrants that its software and firmware designated by VTI for use with a product will execute its programming when properly installed on that product. VTI does not however warrant that the operation of the product, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The warranty shall not apply to defects resulting from improper or inadequate maintenance by the buyer, buyer-supplied products or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

VXI Technology, Inc. shall not be liable for injury to property other than the goods themselves. Other than the limited warranty stated above, VXI Technology, Inc. makes no other warranties, express or implied, with respect to the quality of product beyond the description of the goods on the face of the contract. VTI specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

RESTRICTED RIGHTS LEGEND

Use, duplication, or disclosure by the Government is subject to restrictions as set forth in subdivision (b)(3)(ii) of the Rights in Technical Data and Computer Software clause in DFARS 252.227-7013.

VXI Technology, Inc.
2031 Main Street
Irvine, CA 92614-6509 U.S.A.

DECLARATION OF CONFORMITY

Declaration of Conformity According to ISO/IEC Guide 22 and EN 45014

MANUFACTURER'S NAME	VXI Technology, Inc.
MANUFACTURER'S ADDRESS	2031 Main Street Irvine, California 92614-6509
PRODUCT NAME	VME Switching Modules
MODEL NUMBER(S)	SVM2001, SVM2002B, SVM2003B, SVM2004
PRODUCT OPTIONS	All
PRODUCT CONFIGURATIONS	All

VXI Technology, Inc. declares that the aforementioned products conform to the requirements of the Low Voltage Directive 73/23/EEC *and the* EMC Directive 89/366/EEC *(inclusive* 93/68/EEC*) and carries the "CE" mark accordingly. The products have been designed and manufactured according to the following specifications:*

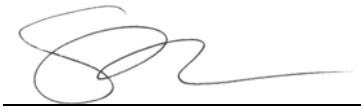
SAFETY	EN61010 (2001)
EMC	EN61326 (1997 w/A1:98) Class A CISPR 22 (1997) Class A VCCI (April 2000) Class A ICES-003 Class A (ANSI C63.4 1992) AS/NZS 3548 (w/A1 & A2:97) Class A FCC Part 15 Subpart B Class A EN 61010-1:2001

The product was installed into a C-size VXI mainframe chassis and tested in a typical configuration.

I hereby declare that the aforementioned products have been designed to be in compliance with the relevant sections of the specifications listed above as well as complying with all essential requirements of the Low Voltage Directive.

March 2007

CE



Steve Mauga, QA Manager

GENERAL SAFETY INSTRUCTIONS

Review the following safety precautions to avoid bodily injury and/or damage to the product. These precautions must be observed during all phases of operation or service of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual, violates safety standards of design, manufacture and intended use of the product.

Service should only be performed by qualified personnel.

TERMS AND SYMBOLS

These terms may appear in this manual:

WARNING Indicates that a procedure or condition may cause bodily injury or death.

CAUTION Indicates that a procedure or condition could possibly cause damage to equipment or loss of data.

These symbols may appear on the product:

ATTENTION - Important safety instructions

Frame or chassis ground

Indicates that the product was manufactured after August 13, 2005. This mark is placed in accordance with *EN 50419, Marking of electrical and electronic equipment in accordance with Article 11(2) of Directive 2002/96/EC (WEEE).* End-of-life product can be returned to VTI by obtaining an RMA number. Fees for take-back and recycling will apply if not prohibited by national law.

WARNINGS

Follow these precautions to avoid injury or damage to the product:

Use Proper Power Cord To avoid hazard, only use the power cord specified for this product.

Use Proper Power Source To avoid electrical overload, electric shock or fire hazard, do not use a power source that applies other than the specified voltage.

Use Proper Fuse To avoid fire hazard, only use the type and rating fuse specified for this product.

WARNINGS (CONT.)

Avoid Electric Shock

To avoid electric shock or fire hazard, do not operate this product with the covers removed. Do not connect or disconnect any cable, probes, test leads, etc. while they are connected to a voltage source. Remove all power and unplug unit before performing any service. ***Service should only be performed by qualified personnel.***

Ground the Product

This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground.

Operating Conditions

To avoid injury, electric shock or fire hazard:

- Do not operate in wet or damp conditions.
- Do not operate in an explosive atmosphere.
- Operate or store only in specified temperature range.
- Provide proper clearance for product ventilation to prevent overheating.
- DO NOT operate if any damage to this product is suspected. ***Product should be inspected or serviced only by qualified personnel.***

Improper Use

The operator of this instrument is advised that if the equipment is used in a manner not specified in this manual, the protection provided by the equipment may be impaired. Conformity is checked by inspection.

SUPPORT RESOURCES

Support resources for this product are available on the Internet and at VXI Technology customer support centers.

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Visit http://www.vxitech.com for worldwide support sites and service plan information.

SECTION 1

INTRODUCTION

INTRODUCTION

The SVM Series leverages off VXI Technology's line of high-density modular VXIbus switches, but optimized for the VMEbus. All SVM switch modules are designed to provide all the features of intelligent switching systems found on other platforms such as GPIB or VXI. These features are achieved in hardware, rather than in a driver or via on-board microprocessor based firmware. This approach to the interface design guarantees the user that all communications to the switch occur in microseconds, as opposed to several milliseconds, considerably improving system throughput.

The SVM series design approach allows virtually any of VXI Technology's SMIP *II*™ product family to be migrated into VME very quickly and cost effectively. The series has been introduced with four common switch modules that provide switching solutions for power, dc, signal, and RF applications. Consult factory for alternative configurations.

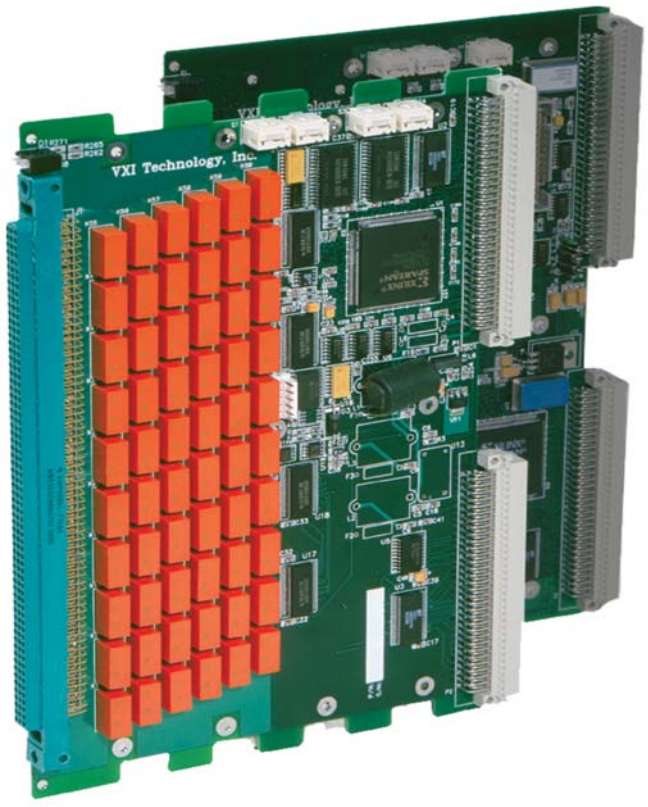

FIGURE 1-1: SVM2001 SWITCH MODULE

DESCRIPTION

All SVM Series modules have a protective, conformal coating applied to it to ensure that the effects of environmental hazards are minimized. This coating endows the modules with resistance to salt spray, moisture, dust, sand and explosive environments, as the polymer coating provides a hermetic seal. The modules have also been designed to withstand the stress and rigors of shock and vibration, allowing the module to be deployed in a variety of applications without concern for damage due to the surrounding physical environment. Table 1-1 details the environmental specifications of these modules.

TABLE 1-1: SVM MODULE ENVIRONMENTAL SPECIFICATIONS

SVM ENVIRONMENTAL SPECIFICATIONS	
CLASSIFICATION	MIL-T-28800E Type III, Class 5, Style E or F
TEMPERATURE	Meets functional shock requirements of MIL-T-28800E, Type III, Class 5
OPERATIONAL	-20°C to 65°C
NON-OPERATIONAL	-40°C to 71°C
HUMIDITY	5% to 95% (non-condensing)
ALTITUDE	
OPERATIONAL	Sea level to 15,000 ft (4,570 m)
SUSTAINED STORAGE	Sea level to 40,000 ft (12,190 m)
RANDOM VIBRATION	Three axis, 30 minutes total, 10 minutes per axis
OPERATIONAL	0.27 g rms total from 5.0 Hz to 55.0 Hz
NON-OPERATIONAL	2.28 g rms total from 5.0 Hz to 55.0 Hz
FUNCTIONAL SHOCK	Half sine, 30 g, 11 ms duration
SALT ATMOSPHERE	> 48 hrs operation
SAND AND DUST	> 6 hrs operation in a dust environment of 0.3 g/ft^3 blowing at 1750 ft/min

SVM modules are designed to operate as slave modules in a VME32/64x chassis with access to relays available in A32 space with D16 and D32 data transfer capability. The modules utilize the +5 V and ±12 V inputs from the VME chassis.

FEATURES

The SVM series interface supports direct register control of all relays, the ability to download scan lists with VME interrupt or software trigger advance, and hardware-implemented break-before-make and make-before break switching.

SECTION 2

PREPARATION FOR USE

INTRODUCTION

When the SVM is unpacked from its shipping carton, the contents should include the following items:

(1) SVM Switch Module
(1) SVM Series User's Manual (this manual)

All components should be immediately inspected for damage upon receipt of the unit. Installation instructions for the modules are discussed in Section 4.

The mainframe should be checked to ensure that it is capable of providing adequate power and cooling for the SVM modules. Once it is found that the chassis meets these specifications, the SVM modules should themselves be examined. If the module is found to be in good condition, the base address of the module may be configured. After setting the base address, the SVM module may be installed into an appropriate 6U VMEbus mainframe in any slot other than slot zero.

CALCULATING SYSTEM POWER AND COOLING REQUIREMENTS

It is imperative that the chassis provide adequate power and cooling for this module. Referring to the chassis operation manual, confirm that the power budget for the system (the chassis and all modules installed therein) is not exceeded and that the cooling system can provide adequate airflow at the specified backpressure.

It should be noted that if the chassis cannot provide adequate power to the module, the instrument might not perform to specification or possibly not operate at all. In addition, if adequate cooling is not provided, the reliability of the instrument will be jeopardized and permanent damage may occur. Damage found to have occurred due to inadequate cooling could also void the warranty of the module.

SETTING THE CHASSIS BACKPLANE JUMPERS

Please refer to the chassis operation manual for further details on setting the backplane jumpers.

SETTING THE BASE ADDRESS

The base address of the SVM series modules is determined by using the offset value (OV), set by four rotary switches located on the top edge of the interface card. The switches are labeled with positions 0 through F. The most significant bit is set by the rotary dial at **S4** and corresponds to the A31 position in memory, while the least significant bit is set by **S1** and corresponds to the A16 position. For example, to set the OV to **25**, first convert the decimal number to the hexadecimal value of **0x0019**. Next, set rotary dial S4 to **0**, S3 to **0**, S2 to **1** and S1 to **9**. This value is then multiplied by 0x10000 to get the base address. See Figure 2-2. Two conversion examples are presented on the following pages.

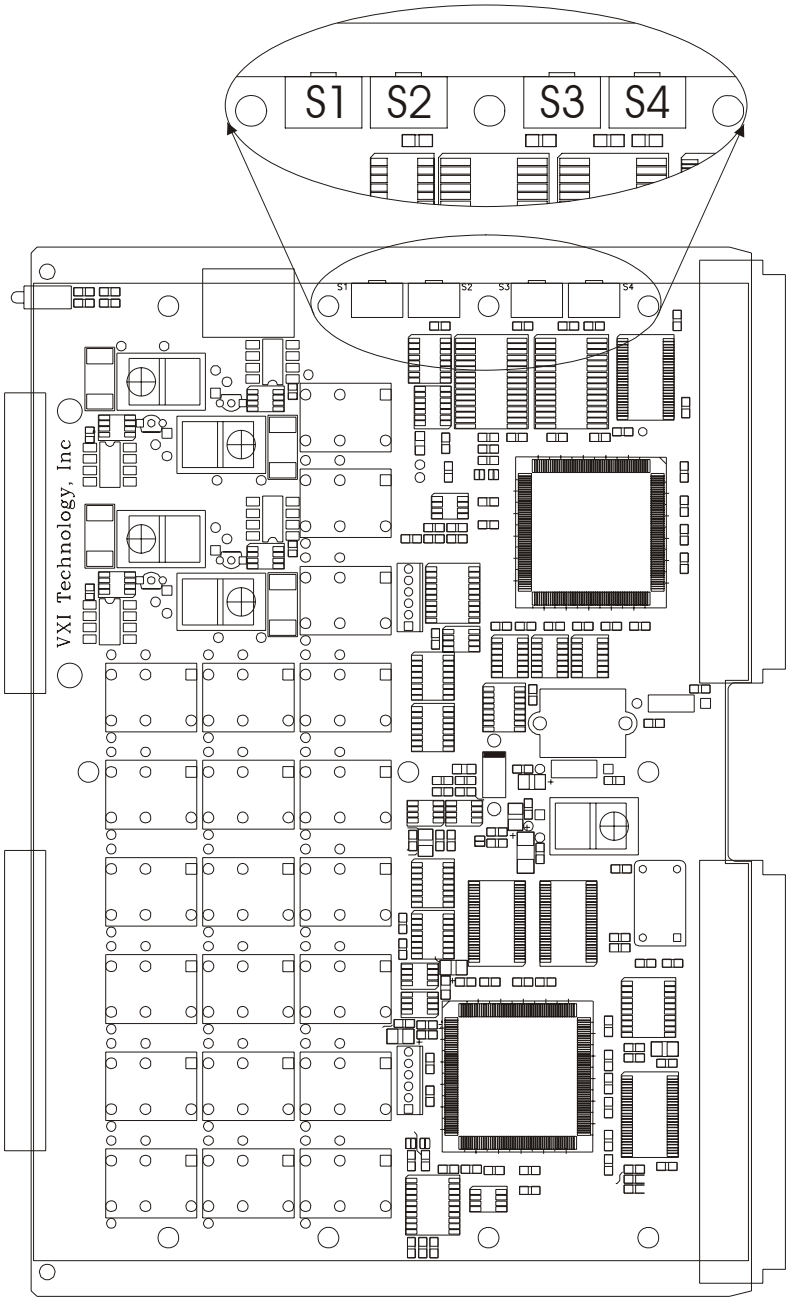

FIGURE 2-1: ROTARY SWITCH LOCATIONS

Example 1

OV (decimal)	Divide by 16^X		S4 (16^3)	S3 (16^2)	S2 (16^1)	S1 (16^0)	
25	25 / 16	=	0	0	1	w/ 9 remainder	*Divide the decimal value by 16 to get the lowest remainder.*
		=	0	0	1	9	*The hexadecimal value. Set switches S4 and S3 to 0, S2 to 1 and S1 to 9.*

Here's another way of looking at the conversion:

OV = (S4 x 4096) + (S3 x 256) + (S2 x 16) + S1
OV = (0 x 4096) + (0 x 256) + (1 x 16) + 9
OV = 0 + 0 +16 + 9
OV = 25

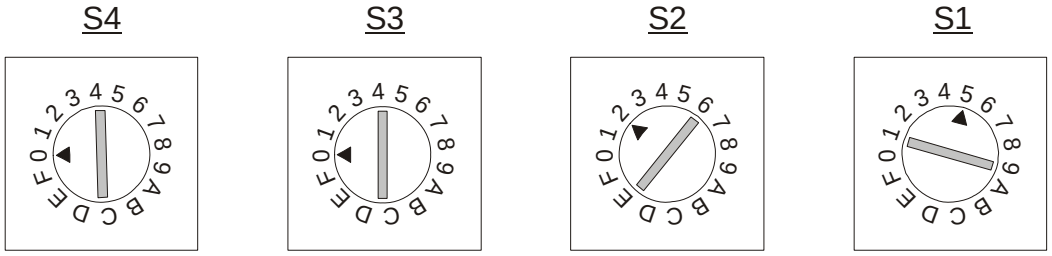

FIGURE 2-2: SWITCH SETTINGS FOR EXAMPLE 1

The base address is then determined by using the following formula:

A32 Base Address = Offset Value * 0x10000 *(or 65,536)*

In this case:

A32 Base Address = 0x19 * 0x10000 *(or 65,536)*
A32 Base Address = 0x00190000

Example 2

In Example 2, the offset value will be set to 4356.

OV (decimal)	Divide by 16^X		S4 (16^3)	S3 (16^2)	S2 (16^1)	S1 (16^0)	
4356	4356 / 4096	=	1	w/ 260 remaining			*Divide the decimal value by 4096 to get the lowest remainder.*
	260 / 256	=	1	1	w/ 4 remaining		*Divide the decimal value by 256 to get the lowest remainder.*
		=	1	1	0	4	*The remainder is smaller than the minimum column value, so it is carried to the next column.*
		=	1	1	0	4	*The hexadecimal value; set S4 to 1, S3 to 1, S2 to 0 and S1 to 4.*

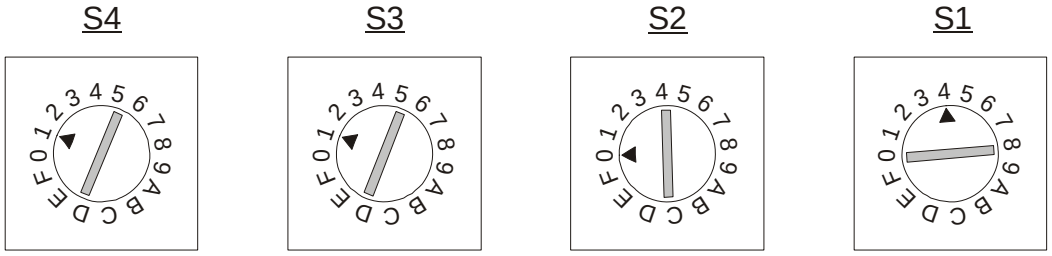

FIGURE 2-3: SWITCH SETTINGS FOR EXAMPLE 2

Therefore, the base address in this example is:

A32 Base Address = 0x1104 * 0x10000 *(or 65,536)*
A32 Base Address = 0x11040000

This information is used to write to the registers of the modules. (See Section 3 for more details on switch module registers. Relay information is provided in Section 4 in each module appendix.)

MODULE INSTALLATION/REMOVAL

Before installing an SVM series switch module into a 6U VME mainframe, make sure that the mainframe is powered down. Insert the module into the base unit by orienting the module so that the flanges at the edge of the module can be inserted into the slot of the base unit. Position the flanges so that they fit into the module slot groove. Once the module is properly aligned, push the module back and firmly insert it into the backplane connector. The retaining screws can then be used to secure the module in the chassis.

To remove the module, power down the mainframe and remove all cabling from the module. The retaining screws can then be loosened. The ejector handles can then be used to assist in the removal of the module.

SECTION 3

PROGRAMMING

PROGRAMMING

The SVM family of switch modules is programmed using direct register access for fast data throughput and boasts the following features for easy programming and integration.

Programmable Timing Delays

A delay can be programmed between relay closures to allow for settling times of other system resources. When used with triggers, a controlled synchronous switching system can easily be configured.

Confidence Checking

Internal feedback provides confidence of relay closures.

Interrupt Driven Triggering

Triggers can be generated when a relay closes and settles and programmed relays can be actuated upon receipt of a trigger to allow for synchronization between other devices. Since trigger management is performed in hardware, triggers command a relay to open or close within microseconds, as opposed to several milliseconds from other competing systems that support triggers.

Make-Before-Break and Break-Before-Make

This feature allows automatic Break-Before-Make (BBM) and Make-Before-Break (MBB) operations. It is programmed simply by setting user configurable options. In BBM operation, all opening relays are guaranteed to open prior to any closing relays being set. The relay open or close time is user configurable as well. In MBB operation, the closing relays are guaranteed to be set prior to the opening relays being opened. These options ease software burden and considerably improves the system.

Safety Interrupt

This is a programmable fail-safe feature that allows all relays to open based upon external or TTL backplane triggers. This allows signals to be removed from the unit under test if a system fail-safe occurs, such as inadvertent removal of a test adapter.

Non-Volatile Memory

Non-volatile memory allows users to store up to 16 bytes of pertinent information such as maintenance records or last user's ID.

Register Access

The SVM switching modules are VMEbus register-based devices for high-speed D16 or D32 data retrieval. Register-based programming is a series of **reads** and **writes** directly to the switch module registers. This eliminates the time for command parsing thus increasing speed.

Automatic Scanning

A predefined sequence of channels can be programmed into 32 kilobytes (kB) of RAM and can be incremented by software or hardware trigger sources. This approach relieves the host controller from having to tie up the VMEbus backplane when scanning.

TABLE 3-1: SVM REGISTER MAP – A32

OFFSET	WRITE FUNCTION	READ FUNCTION
0x8000 – 0xFFFE	Trace RAM	Trace RAM
0x0418 – 0x7FFE	Reserved	Reserved
0x0416	Trace Advance	Board Busy
0x0414	Trace RAM Control	Trace RAM Control
0x0412	Trace RAM Address LOW	Trace RAM Address LOW
0x0410	Trace RAM Address HIGH	Trace RAM Address HIGH
0x040E	Trace RAM End LOW	Trace RAM End LOW
0x040C	Trace RAM End HIGH	Trace RAM End HIGH
0x040A	Trace RAM Start LOW	Trace RAM Start LOW
0x0408	Trace RAM Start HIGH	Trace RAM Start HIGH
0x0406	NVM Access Register	0x0000
0x0404	Interrupt Control	Interrupt Control
0x0402	Control Register 2	Interrupt Status Register
0x0400	Reserved	ID Register
0x0206 – 0x03FE	Reserved	Reserved
0x0204	Reserved	Hardware Revision Register
0x0202	Delay Register	Delay Register
0x0200	Control Register 1	Control Register 1
0x01F0 – 0x01FE	Reserved for Relay Registers	Reserved for Relay Registers
0x0000 – 0x01EE	Relay Register	Relay Register

DESCRIPTION OF SVM MODULE REGISTERS - A32 MEMORY

Each module contains occupies 64 kB (65536 bytes) of memory as shown in the SVM Register Map for A32 address space. The following describes these registers.

Relay Register (0x0000 – 0x01FF) — Read & Write		
D15 - D10	Relay Registers	The lower 512 bytes of memory space are used for module relay control and/or other system functions. Setting a bit to 1 actuates the respective relay. A read back of these registers will show the current state of the module's relays. See the Relay Register Map for a bit-by-bit description of these registers.

Control Register 1 (0x0200) — Read & Write		
D15 - D10	Unused	Reserved for future use.
D9	Relay Data Read Back Polarity Bit	This bit may be used to invert the relay data read back from the plug-in module. Control, Delay and Status Register read backs are not affected by this bit. 0 = Normal polarity relay data is read back from this module 1 = Inverted polarity relay data is read back from this module P_{on} state = 0 (this should always be written as a "0")
D8	ACFAILN Enable Bit	0 = ACFAILN is enabled to reset this module's relays 1 = ACFAILN is disabled from resetting this module's relays P_{on} state = 0
D7	BBM/MBB Enable Bit	If this bit is set, the relays on this module will be sequenced to affect proper BBM (Break-Before-Make) or MBB (Make-Before-Break) operation. If this bit is not set, the module will process the newly written relay data as immediate data, writing it directly to the relay driver ports. No BBM or MBB sequencing will take place. While this feature is enabled, the initial write to the module will start the delay timer running and begin the BBM or MBB operation. Since the relays are controlled by the 16-bit registers, only the affected 16 relays will perform the BBM/MBB operation. To overcome this fact, any subsequent writes to the module, during the initial delay timer time-out period, will be accepted and processed. In addition, the delay time will be reset and begin counting down again. Once the delay timer has timed-out, indicating that the relays have settled into their BBM/MBB state, writes to the module will not be accepted and may result in a Bus Error depending on the value programmed into the delay timer. This is due to the delay timer being reset at the end of the initial time-out and being used to time the final relay closure into their post BBM/MBB state. The module busy signal will only complete once the final relay closure state is reached. If this bit is set and no value has been loaded into the Delay Register, the plug-in module will act as if this enable bit is not set and load all of the relay drivers with immediate data. 0 = BBM/MBB operation is disabled for this module 1 = BBM/MBB operation is enabled for this module P_{on} state = 0

Control Register 1 (0x0200) — Read & Write (cont.)		
D6	BBM/MBB Select Bit	0 = BBM operation on this plug-in module is selected 1 = MBB operation on this plug-in module is selected P_{on} state = 0
D5	Access LED Error Bit	Lights the Access/Error LED red when activated. 0 = Non-active 1 = Active P_{on} state = 0 (Red Error LED lit)
D4	Unused	Reserved for future use.
D3	Front Panel Open to Relay Reset Enable Bit	0 = Front Panel Open signal is not enabled to reset this module's relays 1 = The Front Panel Open signal is enabled to reset this module's relays P_{on} state = 0
D2	Over-current Fault to Relay Reset Enable Bit	The OC (over-current) Fault signal is available on modules with solid-state relays only. It is an indication that an over-current event has occurred in one of the solid-state switches. By querying the appropriate Relay Register, the switch that caused the OC Fault condition can be determined. See the specific module's appendix to determine the applicability of this OC Fault facility. 0 = The OC Fault signal is not enabled to reset this module's relays 1 = The OC Fault signal is enabled to reset this module's relays P_{on} state = 0
D1	Front Panel Open Signal Polarity Bit	Non-inverted: If set in pulse mode, the Front Panel Open signal will generate a reset pulse on a falling edge. If set in level mode, the Front Panel Open signal will generate a reset signal on a low input signal. Inverted: If set in pulse mode, the Front Panel Open signal will generate a reset pulse on a rising edge. If set in level mode, the Front Panel Open signal will generate a reset signal on a high input signal. 0 = Non-inverted Front Panel Open signal polarity 1 = Inverted Front Panel Open signal polarity P_{on} state = 0
D0	Front Panel Open Signal Operation Select Bit	Pulse mode: An edge seen at the Front Panel Open signal pin will generate a reset pulse that may be used to reset the module's relays. The pulse duration is approximately 400 ns. Level mode: A level present on the Front Panel Open signal pin will generate a reset signal that may be used to reset system relays. This signal will remain active as long as the input is active. On the front panel of most SVM modules, there are two pins for access to the Front Panel Open signal of the module. These are the Front Panel Open signal pin (FP-OPEN) and a ground reference pin (FP-GND). The purpose of the Front Panel Open signal is to allow user access to a configurable interlock feature that will reset all of the SVM module's relays. The Front Panel Open signal is intended to be driven by either a switch closure or TTL/CMOS logic gate. It is pulled high on the module. 0 = Pulse mode 1 = Level mode P_{on} state = 0

Delay Register (0x0202) — Read & Write		
D15 - D0	Data Bus 16-bit	This register is used to set the time that the module will hold the Board Busy signal active. The Board Busy signal is set every time the plug-in receives a Write to a relevant Relay Register memory space. The Board Busy signal will be removed at the end of the time out that is set by the value contained in this register. For each count loaded into this register, the Board Busy signal will be held active for approximately 1 μs. The delay may be set from 0 to approximately 65 ms, thus accommodating a wide variation in test station requirements.

Status Register (0x0204) — Read Only		
D15 - D13	Hardware Revision Code	Used to indicate major revisions to the modules hardware.
D12 – D0	Unused	Reserved for future use.

ID Register (0x0400) — Read Only		
D15 - D14	Device Class	Extended register based device, set to 01_2
D13 - D12	Address Space	A32 = 01_2
D11 - D0	Manufacturer's ID	VXI Technology, Inc., set to $F4B_{16}$

Control Register 2 (0x0402) — Write Only		
D15 – D3	Reserved	Writes to these bits have no effect.
D2	Fail LED Control	0 = Front Panel FAIL LED is turned off, non-illuminated. 1 = Front Panel FAIL LED is set on, illuminated RED. P_{on} = 0
D1	Relay Reset Bit	1 = Forces the registers and all relays on the module into a reset state 0 = Releases this soft reset state P_{on} = 0 **Note**: This resets all of the relays on the module.
D0	Reset	1 = Forces the registers on the module into a reset state 0 = Releases this soft reset state P_{on} = 0 **Note**: This does not reset relays on the module.

Interrupt Status Register (0x0402) — Read Only		
D15	Scan Function Done Bit	The latest scan list update is complete.
D14	Front Panel Open Active Event	The Front Panel Open signal was activated by this module.
D13	Over-Current Fault Event	An OC Fault Event has occurred on this module.
D12 – D9	Unused	Reserved for future use.
D8	Busy Complete	The programmed busy signal has timed out. This indicates that the relays actuated for that Busy cycle have settled and a measurement may take place.
D7 – D1	Unused	Reserved for future use.
D0	NVM Data Read Back	Reads of this bit read back the serial data stream from the module. See the NVM Access Register for writes to the serial non-volatile memory on the module.

Interrupt Control Register (0x0404) — Read & Write		
D15	Scan Function done mask bit	IRQ generation enable for the Scan Function Complete Event. 0 = Enabled 1 = Disabled P_{on} = 0
D14	Front Panel Open Active Event true mask bit	IRQ generation enable for the Front Panel Open Active Event. 0 = Enabled 1 = Disabled P_{on} = 0
D13 – D9	Unused	Reserved for future use.
D8	Busy Complete	IRQ generation enable for the Board Busy Event. 0 = Enabled 1 = Disabled P_{on} = 0
D6	IH ENA*	The module has no interrupt handler capability; therefore writing a 1 or 0 has no effect. A 1 is always read back for this bit.
D5 - D3	Interrupter IRQ Line	The complement of the value programmed into these three bits reflects the selected IRQ line used by the module. A value of 011_2 would select IRQ4, a value of 000_2 would select IRQ7, and a value of 111_2 would disconnect the IRQ lines. P_{on} = 000
D2 - D0	Handler IRQ Line	The module has no interrupt handler capability; therefore writing to these bits has no effect. A 111_2 is always read back for these bits.
Note that all bits in this register are set to 1 upon receipt of a hard or soft reset.		

NVM Access Register (0x0406) — Write Only		
D15 – D2	Unused	Data written to these bits have no effect.
D1		Serial clock for the module; should be a logic 1 when not used.
D0		Serial data input for the modules; must be a logic 1 when not used.

Trace RAM Start High Register (0x0408) — Read & Write		
D15 - D4	Unused	Data written to these bits have no effect and always read back as 1.
D3 - D0		Sets the four most significant bits of the starting address of the Trace RAM, allowing the available RAM to be divided into multiple traces. For SVM series modules, these bits must be set to 0.

Trace RAM Start Low Register (0x040A) — Read & Write		
D15 - D0		Sets the 16 least significant bits of the starting address of the Trace RAM, allowing the available RAM to be divided into multiple traces. For the SVM series of modules, the most significant bit, D15, must always be set to 1 to allow access to the Trace RAM.

Trace RAM End High Register (0x040C) — Read & Write		
D15 - D4	Unused	Data written to these bits have no effect and always read back as 1.
D3 - D0		Sets the four most significant bits of the ending address of the Trace RAM, allowing the available RAM to be divided into multiple traces. For SVM series modules, these bits must be set to 0.

Trace RAM End Low Register (0x040E) — Read & Write		
D15 - D0		Sets the 16 least significant bits of the ending address of the Trace RAM, allowing the available RAM to be divided into multiple traces. For the SVM series of modules, the most significant bit, D15, must always be set to 1 to allow access to the Trace RAM.

Trace RAM Address HIGH Register (0x0410) — Read & Write		
D15 - D4	Unused	Data written to these bits have no effect and always read back as 1.
D3 - D0		Sets and reads back the four most significant bits of the current address of the Trace RAM, allowing the current trace RAM address to be queried and changed. For SVM series modules, these bits must be set to 0.

Trace RAM Address LOW Register (0x0412) — Read & Write		
D15 - D0		Sets and reads back the sixteen least significant bits of the current address of the Trace RAM, allowing the current trace RAM address to be queried and changed. For the SVM series of modules, the most significant bit, D15, must always be set to 1 to allow access to the Trace RAM.

Trace RAM Control Register (0x0414) — Read & Write		
D15 – D8	Number of Relay Registers Available on Module	Sets the number of words of address space used by the relays on the module. This number is used in Trace Mode to allow the onboard state-machine to update all relay registers used in the Trace setup. The Relay Registers are always updated in order from 0x00 to the number set in this register. Each Trace setup in the Scan List must update the same number of Relay Registers per setup. Therefore, each Trace setup must have equal numbers of entries in the Trace RAM. One entry corresponding to each updated Relay Register.
D7 – D2	Unused	Reserved for future use.
D1	LOOP ENABLE	If enabled, the trace resumes at the start of active RAM and continues from there. If disabled, the trace stops at the end of active RAM and clears the TRACE ENABLE bit. 1 = Enabled 0 = Disabled
D0	TRACE ENABLE	If the LOOP ENABLE bit is set and the end of active trace RAM is reached, this bit will not be reset. 1 = Enabled 0 = Disabled

Trigger Advance Register (0x0416) — Write Only		
D15 - D0		The act of writing to this location causes a Trace Advance event to occur in the module. The specific data written to these bits has no effect.

Trace RAM (0x8000 – 0xFFFE) — Read & Write		
D15 - D0		Trace RAM

DEVICE MEMORY MAPS

REGISTER ADDRESS

In order to read from and write to the SVM Series switch modules, the register address must be determined. This is defined by two quantities: the module base address and the register offset. The module base address is defined by the rotary switches located on the top edge of the interface card (see *Setting the Base Address* in Section 2 for details.) The register offset is defined by the A32 offset which will be written to. The sum of the module base address and the register offset is the register address.

Register Address = Module Base Address + Register Offset

WRITING TO THE REGISTERS

With both D16 and D32 data transfer available, the user can write either 16 or 32 bits of data to the registers. To change the settings of the module, it is only necessary to write a 16- or 32-bit integer to the specified register with the new configuration:

Register Address, **data**

DETERMINING THE REGISTER ADDRESS

A user is operating an SVM2001 and wishes to open relays **K1** through **K10** and close relays **K11** through **K20**. To do this, the register address must be determined. In this example, it will be assumed that the offset value has been set to 0x0019, yielding a base address of 0x00190000. The register offset for relays falls between the range of 0x000 and 0x1FE. The exact value is determined by reading the relay register map for the SVM2001. When writing the first group of sixteen relays of the SVM2001, the register offset value is 0x000, while writing to the second group of sixteen relays occurs at 0x002. The following register addresses will be written to:

For Relays **K1** through **K16**:

Register Address = Module Base Address + Register Offset

= 0x00190000 + 0x000
= 0x00190000

For relays **K17** through **K32**:

Register Address = Module Base Address + Register Offset

= 0x00190000 + 0x002
= 0x00190002

REGISTER DATA TYPE

The module's relay registers are comprised of 16/32-bit registers that control the relay operation and relay status functions. Not all functions defined below are applicable to all SVM switch modules. The several different bit operations that are controlled via the Relay Registers are defined as follows (note that "*x*" represents the number of the relay):

Kx (Relay Set or Reset Bit) — If this bit is a 1, the associated relay is actuated. If this bit is a 0, then the associated relay is de-actuated.

The K*x* Bits are available to read and write functions.

OCx (Over-Current Bit) If this bit is a 1, then the associated relay has experienced an over-current event. The over-current event specifications and operation are defined for each module in the module appendices found in Section 4. If this bit is a 0, then the associated relay has not experienced an over-current event.

The OC*x* Bits are read only.

A Read of the OC*x* Register will reset the OCx bits to 0.

PROGRAMMING VIA VISA

With the introduction of VISA (*Virtual Instrument Software Architecture*), sending a command to a register-based device is as simple as sending a command to a message-based device. Whether the application is graphical or standard, sending commands to the register-based device is just as intuitive. The VISA template for transferring 16-bit data to a register-based device, utilizing A32 memory space, is as follows:

```
viOut16 (Handle, VI_A32_SPACE, Offset, Data)
```

where,

Handle is passed by reference whenever a VISA session to a particular device is opened.
VI_A32_SPACE is defined in the VISA header file.
Offset is the Register Address defined above.
Data is a 16-bit signed integer value representing the data value.

To send the commands from the example above:

```
viOut16 (Handle, VI_A32_SPACE, 0x00190000, 0xFC00)
viOut16 (Handle, VI_A32_SPACE, 0x00190002, 0x000F)
```

VISA is the software architecture standard instituted by the *Plug&Play* Alliance and is at a very high level of communication to a VMEbus device. The same philosophy and simplicity applies if the instrument is being programmed via lower level commands of an API (*Application Programmer's Interface*).

SECTION 4

MODULE APPENDICES

INTRODUCTION

All modules in the SVM family function as independent instruments in the VMEbus chassis, where each relay of each module can be configured independently of all other modules installed in the VMEbus chassis.

Each module has its own front panel with two indicator LEDs. The A/E (Access/Error) LED flashes green when read/write commands are being sent to the module. The P/F (Power/Fail) LED glows green to indicate that the board is receiving power. Both the A/E and P/F LEDs can be programmed to glow red when a fail condition occurs (see *Access LED Error Bit* and *Fail LED Control Bit* in the module register descriptions for more detail).

Module appendices detail the specifics of each individual SVM module, including connector pin locations, signal assignments, relay maps, schematics, and electronic specifications.

PROTECTED RELAYS

Some SVM Series modules contain protected relays. These switch modules are designed for switching dc signals in applications where the UUT and relays need to be protected.

Each optically isolated protected relay on these modules provides short circuit and current overload protection. This feature not only provides protection should a short or overload occur while the relay is on, but will also provide protection should the relay be switched into a short. In either case, the relay will "sense" the short circuit condition and block it.

The table on the following page illustrates the specifications and properties common to protected relay modules.

APPENDIX SVM2001

SVM2001 - 60 SPDT 300 V, 2 A SWITCH

The SVM2001 is part of the SVM family and can be mixed and matched with other SVM modules to configure high-density switching systems. This appendix shows the 201-pin connector, connector assignments, schematic, relay register map, and electrical specifications information for this module.

This switch module is ideal for general-purpose signal switching where individual relays can be used to route signals to/from the unit under test (UUT), or combined externally to form user-defined configurations.

Below is an illustration of the front panel of the SVM2001, indicating connector pin locations.

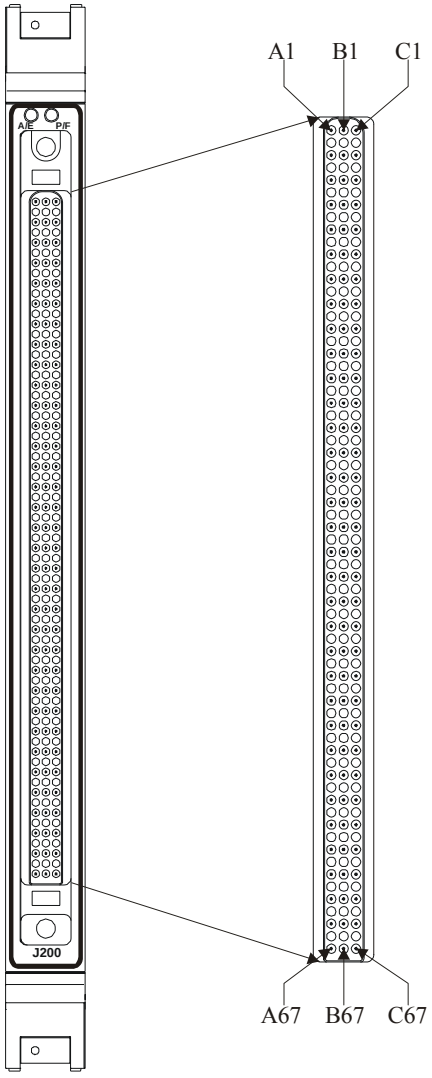

FIGURE 4-1: SVM2001 FRONT PANEL WITH SMB CONNECTORS

TABLE 4-1: SVM2001 CONNECTOR PIN / SIGNAL ASSIGNMENTS

J200					
PIN	**SIGNAL**	**PIN**	**SIGNAL**	**PIN**	**SIGNAL**
A1	SHIELD	B1	FP_OPENN_RTN	C1	FP_OPENN
A2	SHIELD	B2	SHIELD	C2	SHIELD
A3	COM-60	B3	NO-60	C3	NC-60
A4	COM-59	B4	NO-59	C4	NC-59
A5	COM-58	B5	NO-58	C5	NC-58
A6	COM-57	B6	NO-57	C6	NC-57
A7	COM-56	B7	NO-56	C7	NC-56
A8	COM-55	B8	NO-55	C8	NC-55
A9	COM-54	B9	NO-54	C9	NC-54
A10	COM-53	B10	NO-53	C10	NC-53
A11	COM-52	B11	NO-52	C11	NC-52
A12	COM-51	B12	NO-51	C12	NC-51
A13	COM-50	B13	NO-50	C13	NC-50
A14	SHIELD	B14	SHIELD	C14	SHIELD
A15	COM-49	B15	NO-49	C15	NC-49
A16	COM-48	B16	NO-48	C16	NC-48
A17	COM-47	B17	NO-47	C17	NC-47
A18	COM-46	B18	NO-46	C18	NC-46
A19	COM-45	B19	NO-45	C19	NC-45
A20	COM-44	B20	NO-44	C20	NC-44
A21	COM-43	B21	NO-43	C21	NC-43
A22	COM-42	B22	NO-42	C22	NC-42
A23	COM-41	B23	NO-41	C23	NC-41
A24	COM-40	B24	NO-40	C24	NC-40
A25	SHIELD	B25	SHIELD	C25	SHIELD
A26	COM-39	B26	NO-39	C26	NC-39
A27	COM-38	B27	NO-38	C27	NC-38
A28	COM-37	B28	NO-37	C28	NC-37
A29	COM-36	B29	NO-36	C29	NC-36
A30	COM-35	B30	NO-35	C30	NC-35
A31	COM-34	B31	NO-34	C31	NC-34
A32	COM-33	B32	NO-33	C32	NC-33
A33	COM-32	B33	NO-32	C33	NC-32
A34	COM-31	B34	NO-31	C34	NC-31
A35	COM-30	B35	NO-30	C35	NC-30
A36	SHIELD	B36	SHIELD	C36	SHIELD
A37	COM-29	B37	NO-29	C37	NC-29
A38	COM-28	B38	NO-28	C38	NC-28
A39	COM-27	B39	NO-27	C39	NC-27
A40	COM-26	B40	NO-26	C40	NC-26
A41	COM-25	B41	NO-25	C41	NC-25
A42	COM-24	B42	NO-24	C42	NC-24
A43	COM-23	B43	NO-23	C43	NC-23
A44	COM-22	B44	NO-22	C44	NC-22
A45	COM-21	B45	NO-21	C45	NC-21
A46	COM-20	B46	NO-20	C46	NC-20
A47	SHIELD	B47	SHIELD	C47	SHIELD
A48	COM-19	B48	NO-19	C48	NC-19

SVM2001 CONNECTOR PIN / SIGNAL ASSIGNMENTS (CONTINUED)

J200					
PIN	**SIGNAL**	**PIN**	**SIGNAL**	**PIN**	**SIGNAL**
A49	COM-18	B49	NO-18	C49	NC-18
A50	COM-17	B50	NO-17	C50	NC-17
A51	COM-16	B51	NO-16	C51	NC-16
A52	COM-15	B52	NO-15	C52	NC-15
A53	COM-14	B53	NO-14	C53	NC-14
A54	COM-13	B54	NO-13	C54	NC-13
A55	COM-12	B55	NO-12	C55	NC-12
A56	COM-11	B56	NO-11	C56	NC-11
A57	COM-10	B57	NO-10	C57	NC-10
A58	SHIELD	B58	SHIELD	C58	SHIELD
A59	COM-9	B59	NO-9	C59	NC-9
A60	COM-8	B60	NO-8	C60	NC-8
A61	COM-7	B61	NO-7	C61	NC-7
A62	COM-6	B62	NO-6	C62	NC-6
A63	COM-5	B63	NO-5	C63	NC-5
A64	COM-4	B64	NO-4	C64	NC-4
A65	COM-3	B65	NO-3	C65	NC-3
A66	COM-2	B66	NO-2	C66	NC-2
A67	COM-1	B67	NO-1	C67	NC-1

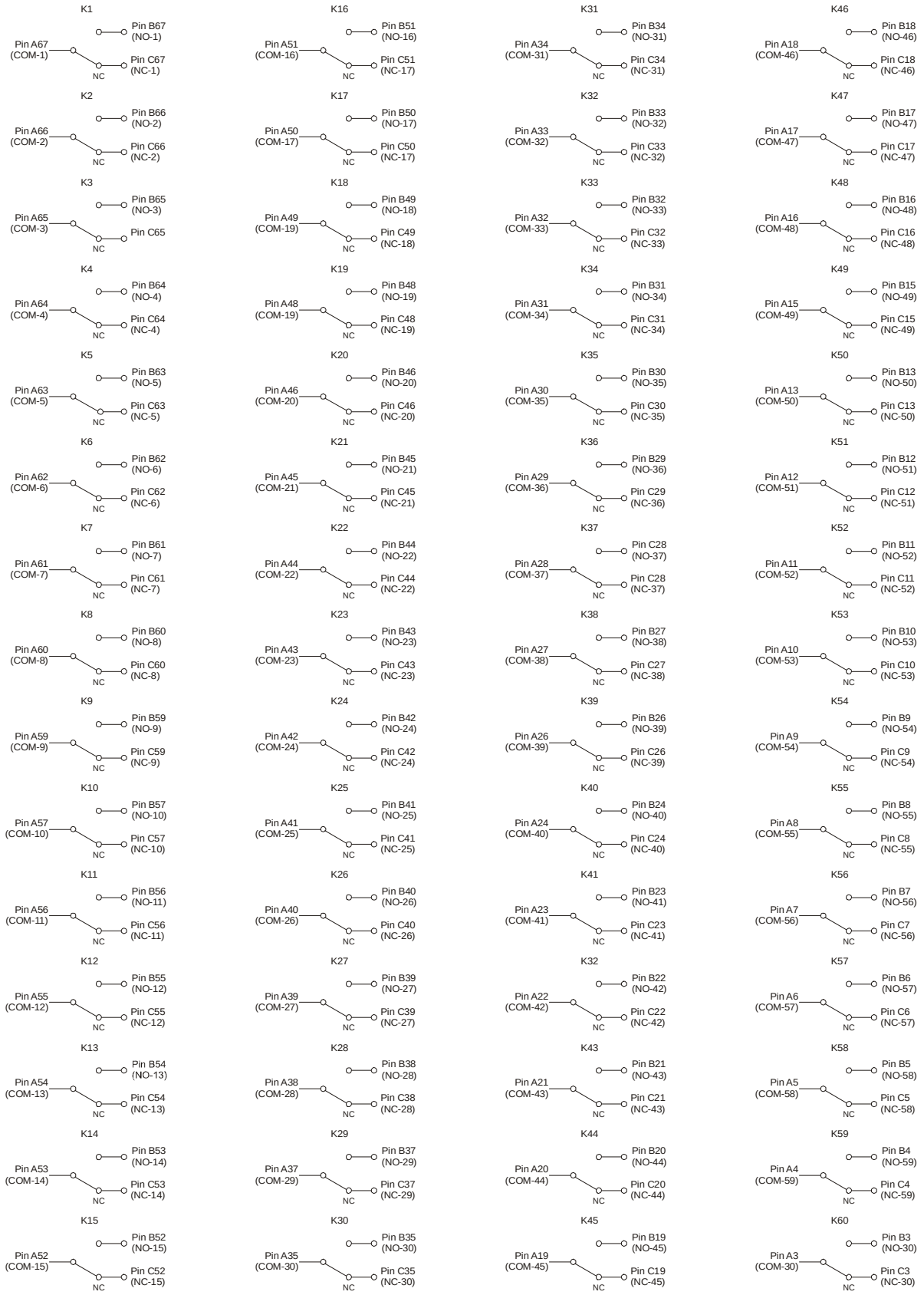

FIGURE 4-2: SVM2001 SCHEMATIC

TABLE 4-2: SVM2001 RELAY REGISTER MAP

Offset (Hex)																
12																
10																
E																
C																
A																
8																
6					K60	K59	K58	K57	K56	K55	K54	K53	K52	K51	K50	K49
4	K48	K47	K46	K45	K44	K43	K42	K41	K40	K39	K38	K37	K36	K35	K34	K33
2	K32	K31	K30	K29	K28	K27	K26	K25	K24	K23	K22	K21	K20	K19	K18	K17
0	K16	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1

SVM2001 SPECIFICATIONS

GENERAL SPECIFICATIONS	
MODEL TYPE	General Purpose
CHANNELS	60 SPDT
VMEBUS INTERFACE	Slave
Address Mode	A32
Data Transfer Mode	D16 or D32
SWITCHING TIME	< 3 ms
RATED SWITCH OPERATIONS	
Mechanical	1×10^7
Electrical	5×10^5 (Full Load)
MTBF	80,000 hrs *(Assumes 20% ground mobile / 80% ground fixed at +52°C ambient or greater)*
POWER SPECIFICATIONS	
MAXIMUM SWITCHING VOLTAGE	300 V ac rms, 300 V dc
MAXIMUM SWITCHING CURRENT	2 A
MAXIMUM SWITCHING POWER	60 W dc, 125 VA
DC PERFORMANCE	
CAPACITANCE	
Open Channel	< 50 pF
Channel-Mainframe	< 80 pF
High-Low	< 50 pF
AC PERFORMANCE	
BANDWIDTH	20 MHz
INSERTION LOSS	
100 kHz	< 0.1 dB
1 MHz	< 0.2 dB
10 MHz	< 1.0 dB
CROSS TALK	
100 kHz	< -80 dB
1 MHz	< -60 dB
10 MHz	< -40 dB
ISOLATION	
100 kHz	< -50 dB
1 MHz	< -45 dB
10 MHz	< -40 dB

APPENDIX SVM2002B

SVM2002B - 26 SPST OPTICALLY ISOLATED PROTECTED 5 A DC SWITCHES

The SVM2002B is part of the SVM family and can be mixed and matched with other SVM modules to configure high-density switching systems. This appendix shows the two 41-pin connectors, connector assignments, schematic, relay register map, and electrical specifications information for this module.

The solid-state switches on this module are isolated and unipolar. They may be used as either high-side or low-side switches. The IN+ input must always be held more positive than the IN- input. These relays incorporate over-current protection.

Below is an illustration of the front panel of the SVM2002B, indicating connector pin locations.

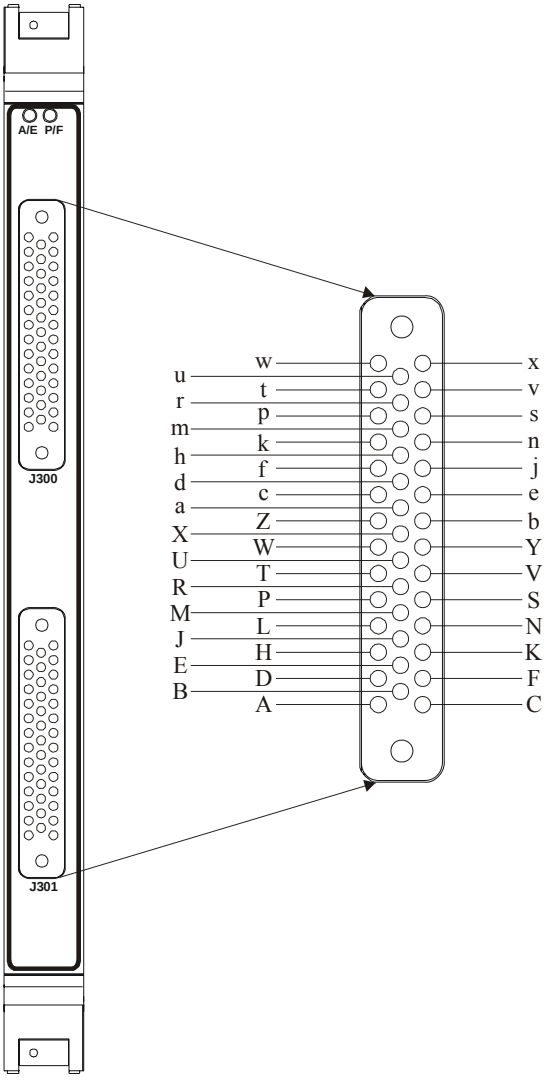

FIGURE 4-3: SVM2002B FRONT PANEL WITH SMB CONNECTORS

TABLE 4-3: SVM2002B CONNECTOR PIN / SIGNAL ASSIGNMENTS

J301		J300	
PIN	**SIGNAL**	**PIN**	**SIGNAL**
A	SHIELD	A	FP_OPENN
B	SHIELD	B	FP_OPENN_RTN
C	IN+ -1	C	IN+ -14
D	IN- -1	D	IN- -14
E	SHIELD	E	SHIELD
F	IN+ -2	F	IN+ -15
H	IN- -2	H	IN- -15
J	SHIELD	J	SHIELD
K	IN+ -3	K	IN+ -16
L	IN- -3	L	IN- -16
M	SHIELD	M	SHIELD
N	IN+ -4	N	IN+ -17
P	IN- -4	P	IN- -17
R	SHIELD	R	SHIELD
S	IN+ -5	S	IN+ -18
T	IN- -5	T	IN- -18
U	SHIELD	U	SHIELD
V	IN+ -6	V	IN+ -19
W	IN- -6	W	IN- -19
X	SHIELD	X	SHIELD
Y	IN+ -7	Y	IN+ -20
Z	IN- -7	Z	IN- -20
a	SHIELD	a	SHIELD
b	IN+ -8	b	IN+ -21
c	IN- -8	c	IN- -21
d	SHIELD	d	SHIELD
e	IN+ -9	e	IN+ -22
f	IN- -9	f	IN- -22
h	SHIELD	h	SHIELD
j	IN+ -10	j	IN+ -23
k	IN- -10	k	IN- -23
m	SHIELD	m	SHIELD
n	IN+ -11	n	IN+ -24
p	IN- -11	p	IN- -24
r	SHIELD	r	SHIELD
s	IN+ -12	s	IN+ -25
t	IN- -12	t	IN- -25
u	SHIELD	u	SHIELD
v	IN+ -13	v	IN+ -26
w	IN- -13	w	IN- -26
x	SHIELD	x	SHIELD

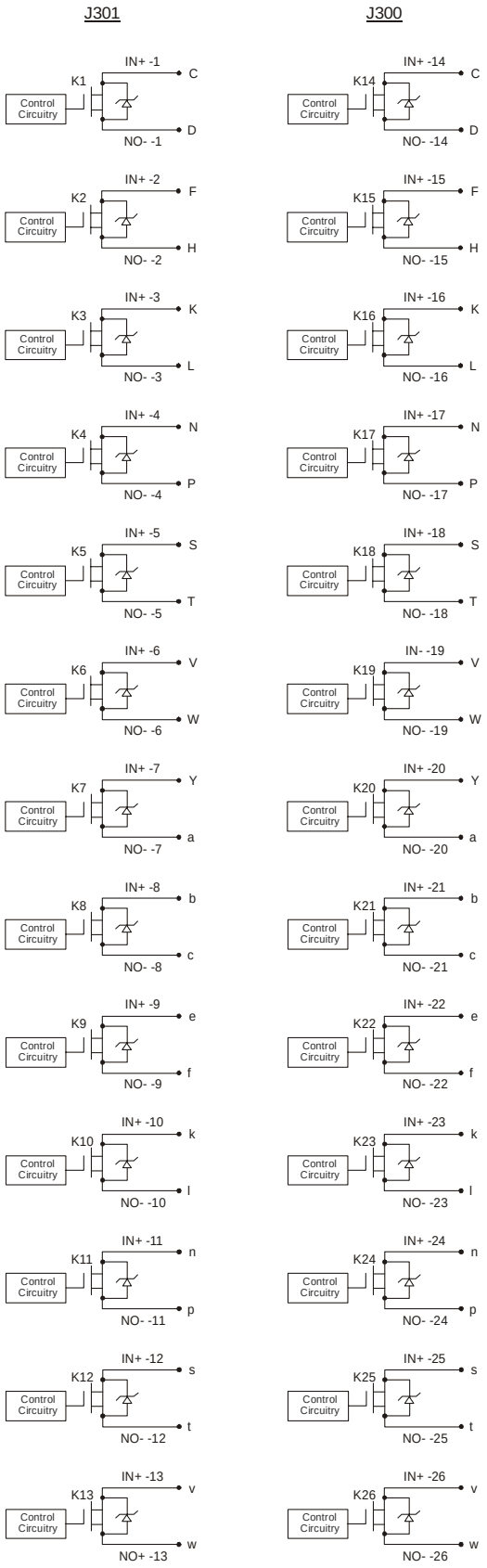

FIGURE 4-4: SVM2002B SCHEMATIC

TABLE 4-4: SVM2002B RELAY REGISTER MAP

Offset (Hex)																
12																
10																
E																
C																
A																
8																
6							OC 26	OC 25	OC 24	OC 23	OC 22	OC 21	OC 20	OC 19	OC 18	OC 17
4	OC 16	OC 15	OC 14	OC 13	OC 12	OC 11	OC 10	OC 9	OC 8	OC 7	OC 6	OC 5	OC 4	OC 3	OC 2	OC 1
2							K26	K25	K24	K23	K22	K21	K20	K19	K18	K17
0	K16	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1

Over-Current Bit (OCx) Operation

If an over-current bit (OCx) is set to "1", the associated relay has experienced an over-current event. If this bit is set to "0", then the associated relay has not experienced an over-current event. For example, if a read of OC1 returns a "1", this indicates that K1 has experienced an over-current event. Note that the OC*x* bits are read only and that a read of the OC*x* register resets the bits to "0".

The OC*x* bit is level-sensitive and will be set anytime an over-current condition exists while the switch is commanded closed. Once set, the OC*x* bit will remain set until a read of the OC*x* register has taken place, even if the over-current condition had previously been removed. If, however, the over-current condition has not been removed, then the over-current detection circuitry will sample the over-current condition and continuously set the OC*x* bit upon each sample that indicates the fault condition.

An over-current condition automatically causes the relay to open. Periodically the relay will try closing and, if it senses an over current condition, it will open again. This is repeated until the over-current condition is removed or the relay is commanded to open.

The OC*x* bit being set does not disable control of the relay.

SVM2002B SPECIFICATIONS

GENERAL SPECIFICATIONS	
MODEL TYPE	Protected Relays
CHANNELS	26 SPST
VMEBUS INTERFACE	Slave
Address Mode	A32
Data Transfer Mode	D16 or D32
SWITCHING TIME	< 1 ms
MTBF	80,000 hrs *(Assumes 20% ground mobile / 80% ground fixed at +52°C ambient or greater)*
POWER SPECIFICATIONS	
MAXIMUM SWITCHING VOLTAGE	35 V dc, unipolar (IN+ = Positive Voltage, IN- = Negative Voltage)
BREAK DOWN VOLTAGE	60 V dc
MAXIMUM SWITCHING CURRENT	5 A
MAXIMUM SWITCHING POWER	175 W dc
DC PERFORMANCE	
ON RESISTANCE	< 150 mΩ
LEAKAGE CURRENT	≤ 10 µA maximum
PROTECTION	
OVER-CURRENT	
Minimum	> 6 A
Maximum	< 7.5 A
SHORT CIRCUIT CURRENT - I_{SC}	Unlimited, but duration clamped by design (Typical: < 2 ms)

APPENDIX SVM2003B

SVM2003B – 100 SPST OPTICALLY ISOLATED PROTECTED 2 A DC SWITCHES

The SVM2003B is part of the SVM family and can be mixed and matched with other SVM modules to configure high-density switching systems. This appendix shows the 201-pin connector, connector assignments, schematic, relay register map, and electrical specifications information for this module.

The solid-state switches on this module are isolated and unipolar. They may be used as either high-side or low-side switches. The IN+ input must always be held more positive than the IN- input. These relays incorporate over-current protection.

Below is an illustration of the front panel of the SVM2003B, indicating connector pin locations.

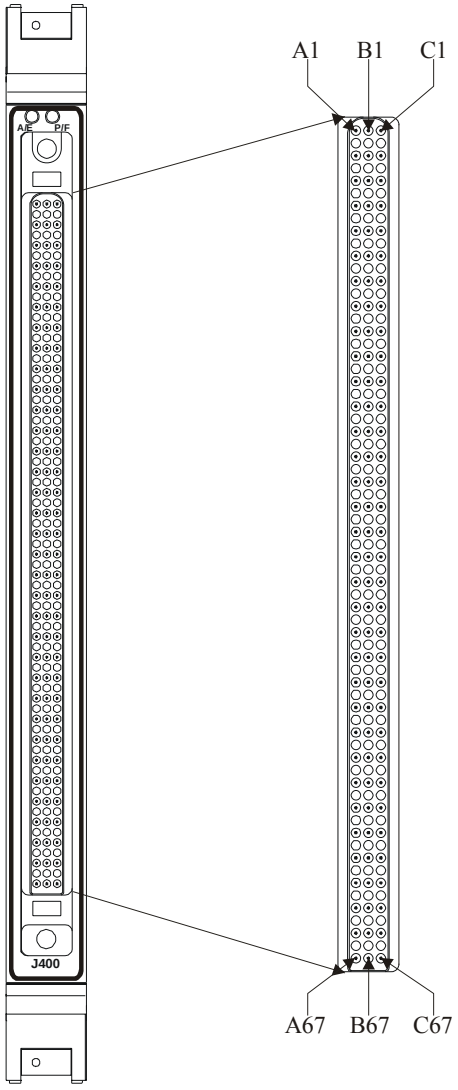

FIGURE 4-5: SVM2003B FRONT PANEL WITH SMB CONNECTORS

TABLE 4-5: SVM2003B CONNECTOR PIN / SIGNAL ASSIGNMENTS

J400					
PIN	**SIGNAL**	**PIN**	**SIGNAL**	**PIN**	**SIGNAL**
A1	IN+ -1	B1	IN- -1	C1	IN+ -2
A2	IN- -3	B2	IN+ -3	C2	IN- -2
A3	IN+ -4	B3	IN- -4	C3	IN+ -5
A4	IN- -6	B4	IN+ -6	C4	IN- -5
A5	IN+ -7	B5	IN- -7	C5	IN+ -8
A6	IN- -9	B6	IN+ -9	C6	IN- -8
A7	IN+ -10	B7	IN- -10	C7	IN+ -11
A8	IN- -12	B8	IN+ -12	C8	IN- -11
A9	IN+ -13	B9	IN- -13	C9	IN+ -14
A10	IN- -15	B10	IN+ -15	C10	IN- -14
A11	IN+ -16	B11	IN- -16	C11	IN+ -17
A12	IN- -18	B12	IN+ -18	C12	IN- -17
A13	IN+ -19	B13	IN- -19	C13	IN+ -20
A14	IN- -21	B14	IN+ -21	C14	IN- -20
A15	IN+ -22	B15	IN- -22	C15	IN+ -23
A16	IN- -24	B16	IN+ -24	C16	IN- -23
A17	IN+ -25	B17	IN- -25	C17	IN+ -26
A18	IN- -27	B18	IN+ -27	C18	IN- -26
A19	IN+ -28	B19	IN- -28	C19	IN+ -29
A20	IN- -30	B20	IN+ -30	C20	IN- -29
A21	IN+ -31	B21	IN- -31	C21	IN+ -32
A22	IN- -33	B22	IN+ -33	C22	IN- -32
A23	IN+ -34	B23	IN- -34	C23	IN+ -35
A24	IN- -36	B24	IN+ -36	C24	IN- -35
A25	IN+ -37	B25	IN- -37	C25	IN+ -38
A26	IN- -39	B26	IN+ -39	C26	IN- -38
A27	IN+ -40	B27	IN- -40	C27	IN+ -41
A28	IN- -42	B28	IN+ -42	C28	IN- -41
A29	IN+ -43	B29	IN- -43	C29	IN+ -44
A30	IN- -45	B30	IN+ -45	C30	IN- -44
A31	IN+ -46	B31	IN- -46	C31	IN+ -47
A32	IN- -48	B32	IN+ -48	C32	IN- -47
A33	IN+ -49	B33	IN- -49	C33	IN+ -50
A34	IN- -51	B34	IN+ -51	C34	IN- -50
A35	IN+ -52	B35	IN- -52	C35	IN+ -53
A36	IN- -54	B36	IN+ -54	C36	IN- -53
A37	IN+ -55	B37	IN- -55	C37	IN+ -56
A38	IN- -57	B38	IN+ -57	C38	IN- -56
A39	IN+ -58	B39	IN- -58	C39	IN+ -59
A40	IN- -60	B40	IN+ -60	C40	IN- -59
A41	IN+ -61	B41	IN- -61	C41	IN+ -62
A42	IN- -63	B42	IN+ -63	C42	IN- -62
A43	IN+ -64	B43	IN- -64	C43	IN+ -65
A44	IN- -66	B44	IN+ -66	C44	IN- -65
A45	IN+ -67	B45	IN- -67	C45	IN+ -68
A46	IN- -69	B46	IN+ -69	C46	IN- -68
A47	IN+ -70	B47	IN- -70	C47	IN+ -71
A48	IN- -72	B48	IN+ -72	C48	IN- -71
A49	IN+ -73	B49	IN- -73	C49	IN+ -74

SVM2003B CONNECTOR PIN / SIGNAL ASSIGNMENTS (CONTINUED)

J400					
PIN	**SIGNAL**	**PIN**	**SIGNAL**	**PIN**	**SIGNAL**
A50	IN- -75	B50	IN+ -75	C50	IN- -74
A51	IN+ -76	B51	IN- -76	C51	IN+ -77
A52	IN- -78	B52	IN+ -78	C52	IN- -77
A53	IN+ -79	B53	IN- -79	C53	IN+ -80
A54	IN- -81	B54	IN+ -81	C54	IN- -80
A55	IN+ -82	B55	IN- -82	C55	IN+ -83
A56	IN- -84	B56	IN+ -84	C56	IN- -83
A57	IN+ -85	B57	IN- -85	C57	IN+ -86
A58	IN- -87	B58	IN+ -87	C58	IN- -86
A59	IN+ -88	B59	IN- -88	C59	IN+ -89
A60	IN- -90	B60	IN+ -90	C60	IN- -89
A61	IN+ -91	B61	IN- -91	C61	IN+ -92
A62	IN- -93	B62	IN+ -93	C62	IN- -92
A63	IN+ -94	B63	IN- -94	C63	IN+ -95
A64	IN- -96	B64	IN+ -96	C64	IN- -95
A65	IN+ -97	B65	IN- -97	C65	IN+ -98
A66	IN- -99	B66	IN+ -99	C66	IN- -98
A67	IN+ -100	B67	IN- -100	C67	SHIELD

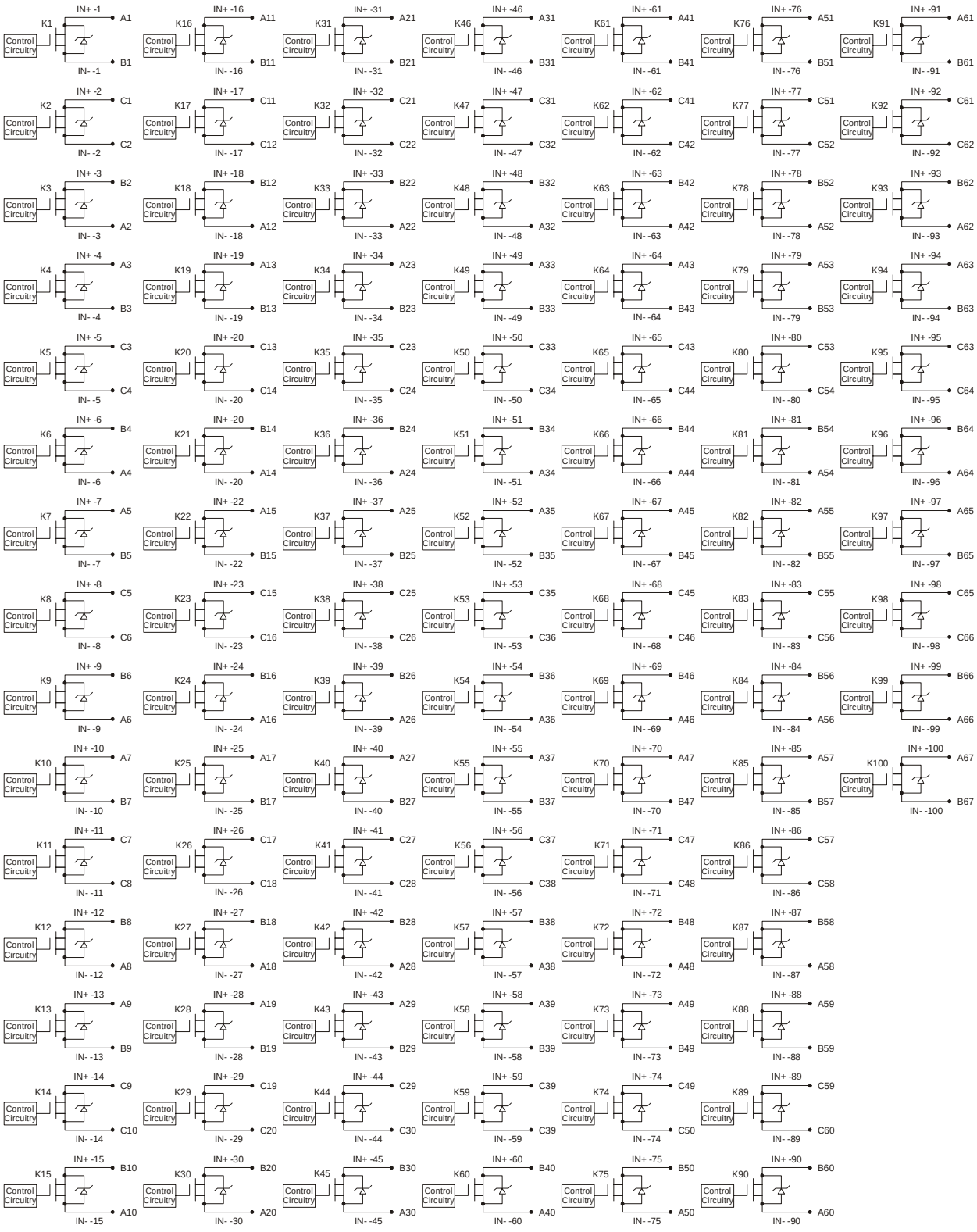

FIGURE 4-6: SVM2003B SCHEMATIC

TABLE 4-6: SVM2003B RELAY REGISTER MAP

Offset (Hex)																
26													OC 100	OC 99	OC 98	OC 97
24																
22																
20																
1E																
1C																
1A																
18	OC 96	OC 95	OC 94	OC 93	OC 92	OC 91	OC 90	OC 89	OC 88	OC 87	OC 86	OC 85	OC 84	OC 83	OC 82	OC 81
16	OC 80	OC 79	OC 78	OC 77	OC 76	OC 75	OC 74	OC 73	OC 72	OC 71	OC 70	OC 69	OC 68	OC 67	OC 66	OC 65
14	OC 64	OC 63	OC 62	OC 61	OC 60	OC 59	OC 58	OC 57	OC 56	OC 55	OC 54	OC 53	OC 52	OC 51	OC 50	OC 49
12	OC 48	OC 47	OC 46	OC 45	OC 44	OC 43	OC 42	OC 41	OC 40	OC 39	OC 38	OC 37	OC 36	OC 35	OC 34	OC 33
10	OC 32	OC 31	OC 30	OC 29	OC 28	OC 27	OC 26	OC 25	OC 24	OC 23	OC 22	OC 21	OC 20	OC 19	OC 18	OC 17
E	OC 16	OC 15	OC 14	OC 13	OC 12	OC 11	OC 10	OC 9	OC 8	OC 7	OC 6	OC 5	OC 4	OC 3	OC 2	OC 1
C													K100	K99	K98	K97
A	K96	K95	K94	K93	K92	K91	K90	K89	K88	K87	K86	K85	K84	K83	K82	K81
8	K80	K79	K78	K77	K76	K75	K74	K73	K72	K71	K70	K69	K68	K67	K66	K65
6	K64	K63	K62	K61	K60	K59	K58	K57	K56	K55	K54	K53	K52	K51	K50	K49
4	K48	K47	K46	K45	K44	K43	K42	K41	K40	K39	K38	K37	K36	K35	K34	K33
2	K32	K31	K30	K29	K28	K27	K26	K25	K24	K23	K22	K21	K20	K19	K18	K17
0	K16	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1

Over-Current Bit (OCx) Operation

If an over-current bit (OCx) is set to "1", the associated relay has experienced an over-current event. If this bit is set to "0", then the associated relay has not experienced an over-current event. For example, if a read of OC1 returns a "1", this indicates that K1 has experienced an over-current event. Note that the OC*x* bits are read only and that a read of the OC*x* register resets the bits to "0".

The OC*x* bit is level-sensitive and will be set anytime an over-current condition exists while the switch is commanded closed. Once set, the OC*x* bit will remain set until a read of the OC*x* register has taken place, even if the over-current condition had previously been removed. If, however, the over-current condition has not been removed, then the over-current detection circuitry will sample the over-current condition and continuously set the OC*x* bit upon each sample that indicates the fault condition.

An over-current condition automatically causes the relay to open. Periodically the relay will try closing and, if it senses an over current condition, it will open again. This is repeated until the over-current condition is removed or the relay is commanded to open.

The OC*x* bit being set does not disable control of the relay.

SVM2003B SPECIFICATIONS

GENERAL SPECIFICATIONS	
MODEL TYPE	Protected Relays
CHANNELS	100 SPST
VMEBUS INTERFACE	Slave
Address Mode	A32
Data Transfer Mode	D16 or D32
SWITCHING TIME	< 1 ms
MTBF	80,000 hrs (*Assumes 20% ground mobile / 80% ground fixed at +52°C ambient or greater)*
POWER SPECIFICATIONS	
MAXIMUM SWITCHING VOLTAGE	35 V dc
MAXIMUM SWITCHING CURRENT	2 A
MAXIMUM SWITCHING POWER	70 W dc
DC PERFORMANCE	
ON RESISTANCE	< 300 mΩ
LEAKAGE CURRENT	≤ 10 µA maximum
PROTECTION	
OVER-CURRENT	
Minimum	> 2.2 A
Maximum	< 7.0 A
SHORT CIRCUIT CURRENT - I_{SC}	Unlimited, but duration clamped by design (Typical < 2 ms)

APPENDIX SVM2004

SVM2004 - 4 SPST OPTICALLY ISOLATED 10 A PROTECTED, 2 SPST 10 A, AND 20 SPDT 5 A SWITCHES

The SVM2004 is part of the SVM family and can be mixed and matched with other SVM modules to configure high-density switching systems. This appendix shows the two 41-pin connectors, connector assignments, schematic, relay register map, and electrical specifications information for this module.

The solid-state switches on this module are isolated and unipolar. They may be used as either high-side or low-side switches. The IN+ input must always be held more positive than the IN- input. The relays incorporate over-current protection.

Below is an illustration of the front panel of the SVM2004, indicating connector pin locations.

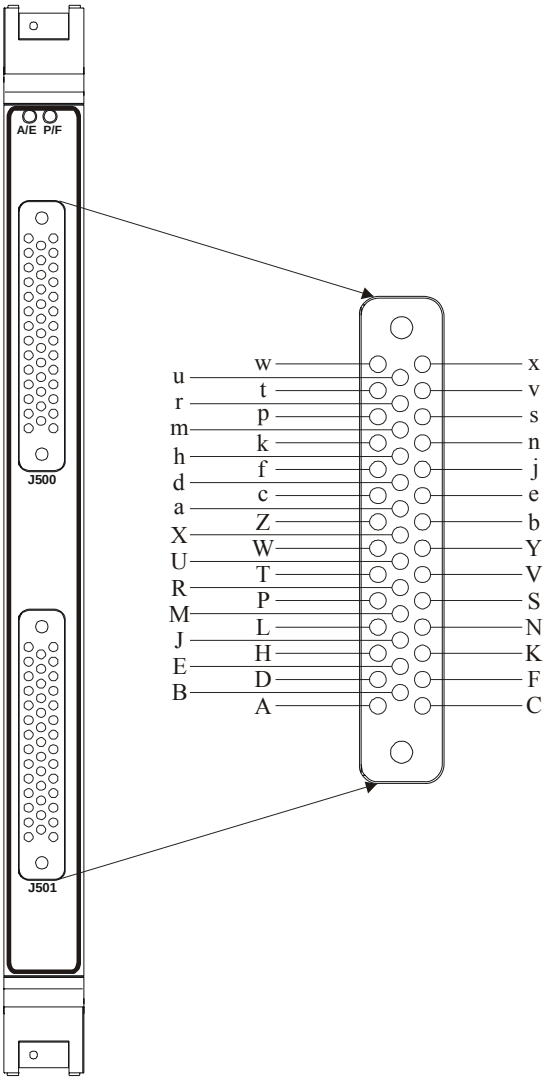

FIGURE 4-7: SVM2004 FRONT PANEL WITH SMB CONNECTORS

TABLE 4-7: SVM2004 CONNECTOR PIN / SIGNAL ASSIGNMENTS

J501		J500	
PIN	SIGNAL	PIN	SIGNAL
A	COM-1	A	COM-13
B	NO-1	B	NO-13
C	NC-1	C	NC-13
D	COM-2	D	COM-14
E	NO-2	E	NO-14
F	NC-2	F	NC-14
H	COM-3	H	COM-15
J	NO-3	J	NO-15
K	NC-3	K	NC-15
L	COM-4	L	COM-16
M	NO-4	M	NO-16
N	NC-4	N	NC-16
P	SHIELD	P	COM-17
R	COM-5	R	NO-17
S	NO-5	S	NC-17
T	NC-5	T	COM-18
U	COM-6	U	NO-18
V	NO-6	V	NC-18
W	NC-6	W	COM-19
X	COM-7	X	NO-19
Y	NO-7	Y	NC-19
Z	NC-7	Z	COM-20
a	COM-8	a	NO-20
b	NO-8	b	NC-20
c	NC-8	c	N/C
d	COM-9	d	FP_OPENN
e	NO-9	e	FP_OPENN_RTN
f	NC-9	f	N/C
h	SHIELD	h	IN- -26 (SS)
j	COM-10	j	IN+ -26 (SS)
k	NO-10	k	IN- -25 (SS)
m	NC-10	m	IN+ -25 (SS)
n	COM-1	n	IN- -24 (SS)
p	NO-11	p	IN+ -24 (SS)
r	NC-11	r	IN- -23 (SS)
s	COM-12	s	IN+ -23 (SS)
t	NO-12	t	NO-22 (10 A)
u	NC-12	u	COM-22 (10 A)
v	SHIELD	v	NO-21 (10 A)
w	SHIELD	w	COM-21 (10 A)
x	N/C	x	N/C

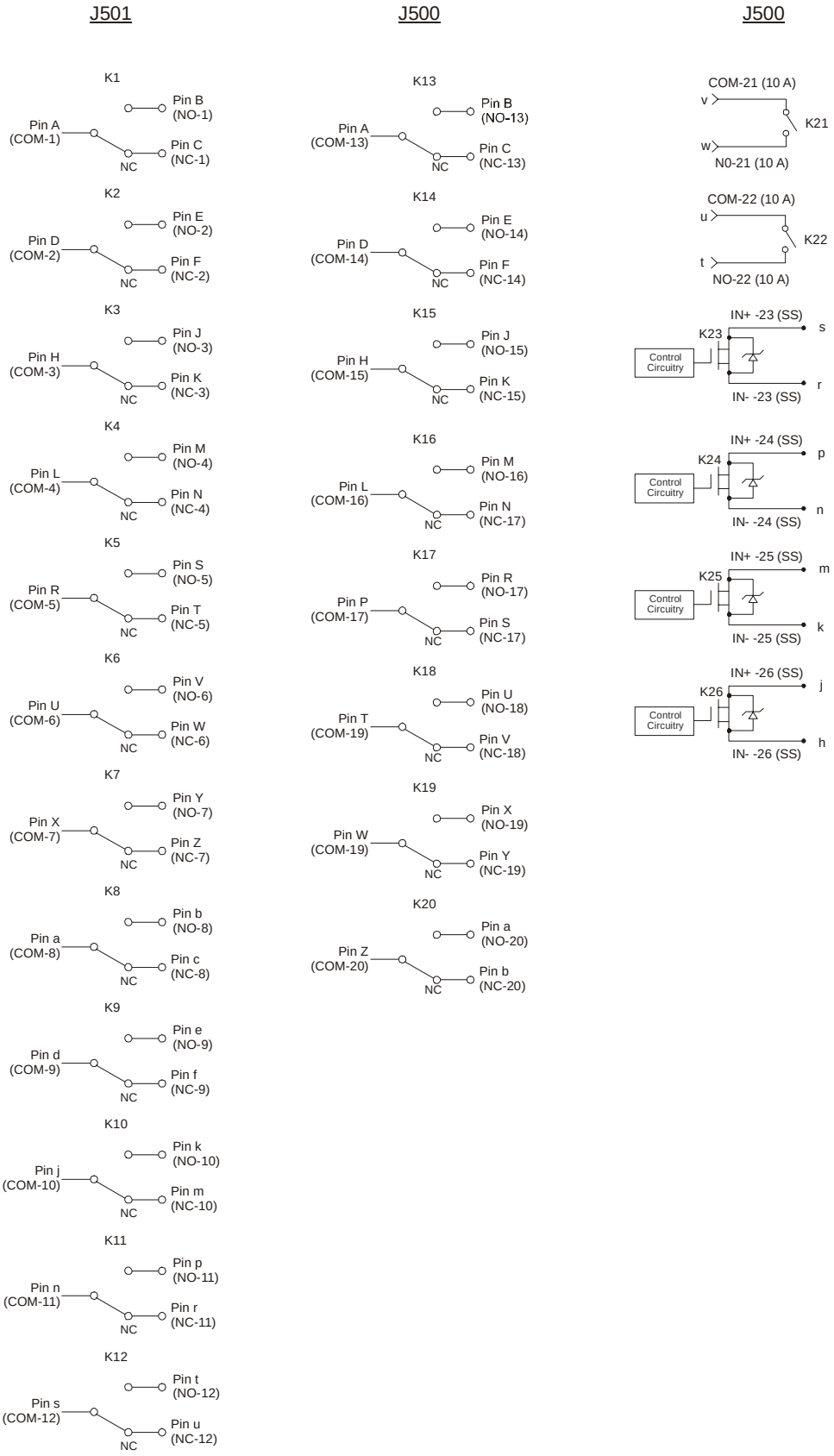

FIGURE 4-8: SVM2004 SCHEMATIC

TABLE 4-8: SVM2004 RELAY REGISTER MAP

Offset (Hex)																
12																
10																
E																
C																
A																
8																
6													OC 26	OC 25	OC 24	OC 23
4													K26 SS	K25 SS	K24 SS	K23 SS
2											K22	K21	K20	K19	K18	K17
0	K16	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1

OCx (Over-Current Bit) Operation

If an over-current (OC*x*) bit is set to "1", then the associated relay has experienced an over-current event. If it is set to "0", then the associated relay has not experienced an over-current event. For example, if a read of OC1 returns a "1", this indicates that K1 has experienced an over-current event. Note that the OC*x* bits are read only and that a read of the OC*x* register will reset the bits to "0".

The OC*x* bit is edge-sensitive and is set anytime an over-current condition occurs while the switch is commanded closed once the Power-On Delay has timed out. Once set, the OC*x* bit will remain set until a read of the OC*x* register has taken place, even if the over-current condition had previously been removed.

When the OC*x* bit is set, the relay will automatically open. The OC*x* status register bit is "sticky," and will remain set once an over-current condition is detected. The signal that resets the relay is temporary and is removed once the relay is reset to the open state. This allows normal control of the relay immediately after an over-current event, but allows status information to persist. A read of the OC*x* register should be initiated to reset the OC*x* bit, allowing future detection of over-current events.

SVM2004 SPECIFICATIONS

GENERAL SPECIFICATIONS	
MODEL TYPE	Measurement and Protected Relay
CHANNELS	4 SPST Protected Relays, 20 SPDT & 2 SPST Electromechanical Switches
VMEbus Interface	Slave
Address Mode	A32
Data Transfer Mode	D16 or D32
Switching Time	
Electromechanical	< 3 ms
Solid State	< 1 ms
Rated Switch Operations	
Electromechanical Lifetime	1×10^7
Electromechanical Full Load	5×10^5
MTBF	80,000 hrs *(Assumes 20% ground mobile / 80% ground fixed at +52°C ambient or greater)*
POWER SPECIFICATIONS	
MAXIMUM SWITCHING VOLTAGE	
Electromechanical	300 V ac rms, 300 V dc
Solid State	35 V dc
MAXIMUM SWITCHING CURRENT	
4 SPST SS Relays	10 A
2 SPST Relays	10 A
20 SPDT Relays	5 A
MAXIMUM SWITCHING POWER	
Electromechanical	60 W dc, 125 VA
Solid State	350 W dc
DC PERFORMANCE	
PATH RESISTANCE	
Electromechanical	< 300 mΩ
ON RESISTANCE	
Solid State	< 100 mΩ
LEAKAGE CURRENT	
Solid State	≤ 10 µA maximum (early units had a maximum leakage of 900 µA)
CAPACITANCE	
Open Channel	< 50 pF
Channel-Mainframe	< 80 pF
High-Low	< 50 pF
AC PERFORMANCE (ELECTROMECHANICAL)	
BANDWIDTH	10 MHz
INSERTION LOSS	
100 kHz	< 0.1 dB
1 MHz	< 0.2 dB
10 MHz	< 3.0 dB
CROSS TALK	
100 kHz	< -80 dB
1 MHz	< -60 dB
10 MHz	< -40 dB
ISOLATION	
100 kHz	< -50 dB
1 MHz	< -45 dB
10 MHz	< -40 dB
PROTECTION (SOLID STATE)	
OVER-CURRENT	
Minimum	> 10 A
Maximum	< 15 A
SHORT CIRCUIT CURRENT - I_{SC}	Unlimited, but duration clamped by design (Typical < 2 ms)

NOTE The solid state switch relays **are not reversible**. IN+ should always be at an equal or greater voltage than IN-.

INDEX

V

W